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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,053	03/26/2004	Klaas Bult	51550/LTR/B600	7909

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EXAMINER	
YOUNG, BRIAN K	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,053	BULT ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,6 and 7* is/are rejected.

7)☒ Claim(s) 2-7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2-7 are objected to because of the following informalities: the claims recite "a method of operating an ***analog to digital converter*** (DAC)". Whereas, they should recite "a digital to analog converter". Claim 7 has no period and appears to be incomplete. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2,3,6 and 7 rejected under 35 U.S.C. 102(e) as being anticipated by Tester.

Tester discloses (fig.3) a method of operating digital to analog converter (DAC) comprising: coupling to a matrix (30) of DAC cells a plurality of binary indications (from 48 and 50) that represent a digital value, the binary indications changing at regular intervals; sampling the DAC cells between the regular intervals after the binary indications change; and latching (latches 70) the cells between the regular intervals.

Tester recites (col1, ln.15-40):

"A clock signal is supplied to the current sources to control sampling of the output of the decoder logic. An extensive clock distribution network is employed to distribute the clock to each of the current cells. Relatively high

currents are used to enable high speed clocking and switching of sampling flip-flops. In particular, high currents are used for DAC architectures in which a latch (or flip-flop) is employed within each current source. For example, as the size of a DAC architecture increases (for example from an 8-bit architecture to a 10-bit architecture or to a 12-bit architecture), the number of current sources increases in a power series of 2.sup.x where x is the number of bits. Each time all of the latches are clocked concurrently, a relatively large current spike is produced. The current spike can cause interference between current sources, and necessitates relatively large smoothing capacitors to smooth a power supply to the DAC. The large smoothing capacitors represent additional cost and size implications. Such a large current demand also means that the power consumption is undesirably high.

Tester also recites (col.5, ln.18-65) "In FIG. 3, the arrangement of the group decoder 40 may be schematic in nature, and different circuit or logic configurations and distributions may be used.

The group decoders 40 may be generally comprised of combinational logic, which may not be clocked. The combination logic may provide that the digital word 44, and any changes thereto, may be decoded as quickly as possible. In order to ensure that the groups 30 of first current sources 18 may be maintained in synchronism, ***the row and column signals 54 may be sampled by respective flip-flops 70***. The flip-flops 70 may act as an ***interface to the current sources 18***. Either the flip-flops 70 or the

current sources 18, or both, may form a plurality or array of clockable sub-circuits. The flip-flops may be controlled by respective clock signals 72a-d in each group 30. The clock signals 72a-d may also drive the current sources 18 in each group to ensure that the current sources 18 generally operate in synchronism. Such clocking of the current sources 18 may be desirable to avoid delays or skew caused by variations in signal path lengths along the circuit paths for the row and column control signals 54 to each current source 18, depending on a physical position of the respective current source 18 in the array. A feature may be a provision of a clock controller 74 for controlling the distribution of the clock signals 72a-d to the groups 30a-d. A function of the clock controller 74 may be to determine whether, for each group 30, the row and column signals 54 may have changed since the last clock cycle. For example, if the group 30 was decoded to be either entirely off, or entirely on, in a previous clock cycle, and may be decoded to be in the same state for a current clock cycle, the row and column signals 54 may be considered to be unchanged. Therefore, the clock controller 74 may function to inhibit the clock signal 72 for the determined group 30. Inhibiting the clock signal 72 for one or more entire groups 30 may be advantageous in reducing power consumption, and avoiding unnecessary clocking of the flip-flops 70. Each time the flip-flops 70 are clocked, the flip-flops 70 consume power and there may also be a risk of interference and cross-talk with other circuit elements. A reduction in power consumption may be extremely beneficial, as DACs tend to be relatively inefficient, especially when used at high speeds. Also, a reduction in the current spikes occurring on power supply lines on each clock cycle may enable use of a smaller number and

size of smoothing capacitors for the power supply. Particularly for portable, or battery operated, or miniature electronic devices, smaller filters may be highly desirable. The flip-flops 70 arranged in the row direction may be in the same scan chain as the flip-flops 70 in the column direction (as indicated in FIG. 3), or two different scan chains may be used, one for the column direction and one for the row direction. ***By sequentially clocking values into and/or along the chain, current sources 18 may be turned on and off individually. Thus the circuit performs an "anding" function. Clocking is performed by the "clock" signal shown (fig.3).***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Morita, et al *6,509,854 disclose*** a DA converter wherein an analog output voltage is formed in such a way that constant currents formed by a plurality of constant-current source transistors are selectively fed to a load resistor by controlling switching means to turn ON and OFF in correspondence with input signals; each of the constant-current source transistors is operated in an operating range from a saturation region to a non-saturation region as the output voltage enlarges in its absolute value, and those of the plurality of constant-current source transistors whose currents based on the operations in the non-saturation regions are selected by the switching means have their sizes enlarged so as to compensate for current decrements ascribable to such operations in the non-saturation regions.

Sauerwald *5,084,701 disclose digital*-to-analog (D/A) converter using cyclical current source switching to average out the errors in individual current sources. The D/A

converter includes a current source switching circuit, a bank of constant current sources and a control circuit. The current source switching circuit, which is clocked by the control circuit, generates an upper and a lower pointer in accordance with a digital input signal. The upper pointer, which is advanced for an increasing digital input signal, connects current sources to an output bus. The lower pointer, which is advanced for a decreasing digital input signal, disconnects current source from the output bus. The upper and lower pointers continuously cycle through the bank of current sources to average out the errors in the individual current sources.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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